Remarks

I. Status of claims

Claims 47-60 were pending.

Claims 49 and 56 have been canceled without prejudice.

Claims 61-66 have been added.

II. Claim rejections

A. Claims 47 and 54

The Examiner has rejected claims 47 and 54 under 35 U.S.C. § 102(b) over Ramdani (U.S. 5,835,521). In particular, the Examiner has indicated that claims 47 and 54 are anticipated by the alternative embodiment of Ramdani's VCSEL that is defined by proton implantation (see col. 5, lines 50-52). In this embodiment, the proton-implanted region surrounds the active region 34, the cladding layer 32, the current spreading layer 31 and the contact layer 28. In his rejection, the Examiner has indicated that the proton-implanted region corresponds to the defect source recited in claims 47 and 54 and that the current spreading layer 31 corresponds to the reliability-enhancing layer recited in claims 47 and 54.

Each of claims 47 and 54 has been amended and now recites that the cavity region includes a first side facing the first mirror stack and a second side facing the second mirror stack, and that the defect source is located such that only one of the first and second sides of the cavity region faces the defect source. In the alternative embodiment of Ramdani's VCSEL, the proton-implanted region is not faced by only one of the first and second sides of the active region 34 that face the first and second DBR's 10, 42. Instead, the proton-implanted region surrounds the active region 34.

In addition, each of claims 47 and 54 has been amended to recite that the reliability-enhancing layer is positioned within the defect source to reduce migration of defects in the vertical direction from the defect source to the active region. The portion of the current spreading layer 31 that is within the proton-implanted region is not positioned within the proton-implanted region to reduce migration of defects in the vertical direction from the defect source to the active region.

For at least these reasons, the Examiner's rejection of claims 47 and 54 under 35 U.S.C. § 102(b) over Ramdani now should be withdrawn.

B. Claims 48, 49, 55, and 56

The Examiner has rejected claims 48, 49, 55, and 56 under 35 U.S.C. § 102(b) over Yuen (U.S. 5,991,326). The features of claims 49 and 56 have been incorporated into claims 48 and 55, respectively. Claims 49 and 56 have been canceled without prejudice.

1. Claim 48

In his rejection of claim 48, the Examiner indicated that:

> Yuen discloses the claimed VCSEL (fig.1) comprising a first mirror stack (fig.1 #10), a second mirror stack (fig.1 #32), a cavity region disposed between the first mirror stack and the second mirror stack (fig.1 #16) including an active region (fig. I #20), a defect source (fig.3 #46), and a reliability-enhancing layer (fig.1 #32 bottom layer, when material of type InGaAsP, co1.5 lines 20-21) positioned with respect to the defect source to reduce defect induced degradation of one or more VCSEL regions, where the defect source is disposed between the reliability-enhancing layer and the cavity region (fig.3, oxidized region between InGaAsP mirror layer and cavity region).

In this rejection, however, the Examiner impermissibly has relied on a *single* region in Yuen's VCSEL (namely, top DBR 32) to meet *two* separate elements recited in claim 48 (namely, the second mirror stack and the reliability-enhancing layer). If the Examiner chooses to assert that the top DBR 32 corresponds to the "second mirror stack" recited in claim 48, then the Examiner will have failed to specifically point to a layer in Yuen's VCSEL that corresponds to the "reliability-enhancing layer" recited in claim 48. On the other hand, if the Examiner chooses to assert that top DBR 32 corresponds to the "reliability-enhancing layer" recited in claim 48, then the Examiner will have failed to specifically point to a region in Yuen's VCSEL that corresponds to the "second mirror stack" recited in claim 48; the Examiner also will have failed to identify which of the multiple layers of the top DBR 32 corresponds to the reliability-enhancing layer recited in claim 48.

Thus, the Examiner has failed to establish a proper *prima facie* case of anticipation under 35 U.S.C. § 102(b) over Yuen. For at least this reason, the Examiner's rejection of claim 48 under 35 U.S.C. § 102(b) over Yuen should be withdrawn.

In addition, claim 48 now recites that the VCSEL includes "a second reliability-enhancing layer positioned with respect to the defect source to reduce defect-induced degradation of the active region by the defect source, wherein the second reliability-enhancing layer is separated from the first reliability-enhancing layer by one or more other layers and the first and second reliability-enhancing layers are located on opposite sides of the defect source."

In his rejection of claim 49, the Examiner has indicated that the lattice-matched spacer layer 18 corresponds to the second reliability-enhancing layer. The spacer layer 18, however, is not positioned with respect to the defect source to reduce defect-induced degradation of the active region by the defect source, as now recited in claim 48. Indeed, the spacer layer 18 is positioned below the quantum well region 20 and therefore would not have any influence whatsoever on the degradation of the quantum well region 20 by defects that might be induced by the ion implant region 46.

For at least this additional reason, the Examiner's rejection of claim 48 under 35 U.S.C. § 102(b) over Yuen should be withdrawn.

2. Claim 55

Claim 55 essentially tracks claim 48 and is patentable over Yuen for at least the same reasons explained above.

C. Claims 50-52 and 57-59

1. Claim 50

The Examiner has rejected claim 50 under 35 U.S.C. § 102(b) over Yuen. The Examiner has explained the basis for this rejection as follows (emphasis added):

> Yuen discloses the claimed VCSEL (fig.1) comprising a first mirror stack (fig.1 #10), a second mirror stack (fig.1 #32), a cavity region disposed between the first mirror stack and the

> second mirror stack (fig.1 #16) including an active region (fig.1 #20), a defect source (fig.3 #46), and a reliability enhancing layer (fig.1 #26, col. 4 lines 51-53) positioned with respect to the defect source to reduce defect induced degradation of one or more VCSEL regions, wherein the reliability-enhancing layer is configured to at least in part balance strain created by the defect source (layer 26 is used to prevent lattice mismatch with the quantum well, col.4 lines 54-56, and is located within the strain field of the defect region 46 and inherently performs the strain balancing function because it has the same structure and composition as the instant invention).

In this rejection, however, it appears that the Examiner has misconstrued Yuen's teachings. In particular, Yuen teaches that (col. 4, lines 51-63; emphasis added):

> At least one additional intermediate layer 26 is deposited on top of spacer layer 24. This layer is composed of lattice matched materials, such as InAlGaAs, InGaAsP, AlGaAsSb. Intermediate layer 26 is applied to prevent a lattice mismatched top DBR 32 from affecting the lattice structure of quantum well region 20. Intermediate layer 26 is not needed when spacer 24 is sufficiently thick. For an example, when spacer 24 is 1,800 angstroms, a intermediate layer 26 of 5,000 angstrom is needed. When spacer 24 is 3,000 angstroms, then intermediate layer 26 is not needed. A person of average skill in the art will be able to determine the critical thickness of spacer 24 up to which intermediate layer 26 is necessary without undue experimentation.

Thus, Yuen teaches that the intermediate layer 26 prevents the lattice-mismatched top DBR 32 from affecting the lattice structure of the quantum well by making the intermediate layer 26 sufficiently thick so that the dislocations that occur between the lattice-mismatched portion (i.e., top DBR 32 and current confinement layer 28) do not affect the lattice structure of the quantum well region 20. That is, the intermediate layer 26 separates the quantum well region 20 from the dislocations and other defects that are created by the strain relaxation between the current confinement layer 28 and intermediate layer 26. Yuen does not even hint that the intermediate layer 26 is configured to balance strain created by the ion implant region 46. To the contrary, Yuen teaches that the strain between the lattice-mismatched current confinement layer 28 (in which the ion implant region 46 is formed) and the intermediate layer 26 is relaxed (see col. 5, lines 16-17). Therefore, by definition, there is no strain between these layers 26, 28 and, hence, there is no strain balancing by the intermediate layer 26.

For at least these reasons, the Examiner's rejection of claim 50 under 35 U.S.C. § 102(b) over Yuen should be withdrawn.

The Examiner also has rejected claim 50 under 35 U.S.C. § 102(b) over Duggan (U.S. 5,991,321). In particular, the Examiner has indicated that:

> With respect to claim 50, Duggan discloses the claimed VCSEL (fig.13) comprising a first mirror stack (fig. 13 #28), a second mirror stack (fig. 13 #26), a cavity region disposed between the first mirror stack and the second mirror stack (fig. 13 #I2) including an active region (fig.13 #10), a defect source (fig.13 #30), and a reliability enhancing layer (fig.13 #6, col.8 lines 14-15) positioned with respect to the defect source to reduce defect induced degradation of one or more VCSEL regions, wherein the reliability-enhancing layer is configured to at least in part balance strain created by the defect source (layer 6 is located within the strain field of the defect region 30 and inherently performs the strain balancing function because it has the same structure and composition as the instant invention)

Contrary to the Examiner's assertion, however, the electrically insulating polymer current-confining layer 30 does not create strain in Duggan's VCSEL. Consequently, there is no strain for the electron-reflecting barrier layer 6 to balance.

In addition, even assuming only for the purpose of argument that the electrically insulating polymer current-confining layer 30 introduced some sort of strain in Duggan's VCSEL, the electron-reflecting barrier layer 6 could not balance such strain because the electron-reflecting barrier layer 6 is not adjacent to the electrically insulating polymer current-confining layer 30.

Furthermore, even assuming only for the purpose of argument that the electrically insulating polymer current-confining layer 30 introduced some sort of strain in Duggan's VCSEL, Duggan fails to teach or suggest anything that would have led one of ordinary skill in the art at the time the invention was made to configure the electron-reflecting barrier layer 6 to balance such strain.

For at least this reason, the Examiner's rejection of claim 50 under 35 U.S.C. § 102(b) over Duggan should be withdrawn.

2. Claim 51

Claim 51 incorporates the features of independent claim 50 and therefore is patentable over Yuen and Duggan for at least the same reasons explained above.

3. Claim 52

The Examiner has rejected claim 52 under 35 U.S.C. § 103(a) over Duggan in view of Yuen. In particular, the Examiner has indicated that:

> With respect to claim 52, Dugan teaches the VCSEL outlined in rejection of claim 50 above, comprising the reliability-enhancing layer formed of $In_xGa_{1-x}P$ wherein $x<0.5$ (col.7 lines 13-17), Dugan does not teach one of the first and second mirror stacks to comprise oxidized AlGaAs layers. Yuen teaches DBR layers to be made of oxidized AlGaAs (col.5 lines 20-25). It would have been obvious at the time of the invention to one of ordinary skill in the art to combine the VCSEL of Dugan with the oxidized AlGaAs mirror stack of Yuen to provide a large refractive index difference between the adjacent DBR layers and increase the DBR stop bandwidth and relax the growth accuracy for the DBR (Yuen, col.5 lines 25-32).

As explained above, Duggan teaches that the electron-reflecting barrier layer 6 is formed in the middle of the p-type spacer 16. If one or more of the layers of the p-DBR 26 were oxidized as proposed by the Examiner, the electron-reflecting barrier layer 6 could not balance such strain because the electron-reflecting barrier layer 6 is not adjacent to the electrically insulating polymer current-confining layer 30. Therefore, the Examiner's proposed modification of Duggan's VCSEL would not result in the inventive VCSEL recited in claim 52.

In addition, neither Duggan nor Yuen teaches or suggests anything that would have led one of ordinary skill in the art at the time the invention was made to configure the electron-reflecting barrier layer 6 to balance the strain that might be introduced by the Examiner's proposed modification of Duggan's VCSEL. The Examiner has asserted that in col. 7, lines 13-17, Duggan teaches that the VCSEL shown in FIG. 13 includes a reliability-enhancing layer that is formed of $In_xGa_{1-x}P$ wherein $x<0.5$. In the cited section, Duggan merely teaches that in one embodiment "the barrier layer 6 is made from a non-lattice matched $In_zGa_{1-z}P$ alloy, the value being chosen so that the (InGa)P is under tensile strain

when grown on a GaAs substrate." In the VCSEL shown in FIG. 13, however, the barrier layer 6 is formed in a p-doped (AlGaIn)P spacer region 16. Duggan does not provide any guidance as to the composition of the barrier layer 6 shown in FIG. 13, much less anything about the strain (if any) in the barrier layer shown in FIG. 13.

For at least these reasons, the Examiner's rejection of claim 52 under 35 U.S.C. § 103(a) over Duggan in view of Yuen should be withdrawn.

4. Claim 57

The Examiner has rejected claim 57 under 35 U.S.C. § 102(b) over Yuen. The Examiner also has rejected claim 57 under 35 U.S.C. § 102(b) over Duggan.

Claim 57 essentially tracks claim 50 and therefore is patentable over Yuen and Duggan for at least the same reasons explained above.

5. Claim 58

Claim 58 incorporates the features of independent claim 57 and therefore is patentable over Yuen and Duggan for at least the same reasons.

6. Claim 59

The Examiner has rejected claim 59 under 35 U.S.C. § 103(a) over Duggan in view of Yuen.

Claim 59 essentially tracks claim 52 and therefore is patentable over Yuen and Duggan for at least the same reasons explained above.

D. Claims 53 and 60

The Examiner has rejected claims 53 and 60 under 35 U.S.C. § 102(b) over Yuen. With respect to claim 53, the Examiner has indicated that (emphasis added):

> Yuen discloses the claimed VCSEL (fig.1) comprising a first mirror stack (fig.1 #10))a second mirror stack (fig.1 #32), a cavity region disposed between the first mirror stack and the

> second mirror stack (fig. I #16) including an active region (fig. 1 #20), a defect source (fig.3 #46), and a reliability-enhancing layer (fig. 1 #26, col.4 lines 51-53) positioned with respect to the defect source to reduce defect induced degradation of one or more VCSEL regions, wherein the defect source creates a concentration gradient inducing defect migration, and the reliability-enhancing layer is configured to reduce the induced defect migration (layer 26 inherently reduces defect migration because it has the same structure and composition as the instant invention).

Claim 53 now recites that the reliability-enhancing layer introduces strain that reduces the defect migration introduced by the concentration gradient created by the defect source. Yuen teaches that the strain between the lattice-mismatched current confinement layer 28 (in which the ion implant region 46 is formed) and the intermediate layer 26 is relaxed (see col. 5, lines 16-17). Therefore, by definition, there is no strain between these layers 26, 28. Hence, there is no reasonable basis for one of ordinary skill in the art at the time the invention was made to believe that the intermediate layer 26 constitutes a reliability-enhancing layer that is configured to reduce defect migration induced by a concentration gradient that might be created by the ion implant region.

For at least this reason, the Examiner's rejection of claim 53 under 35 U.S.C. § 102(b) over Yuen should be withdrawn.

Claim 60 essentially tracks claim 53 and therefore is patentable over Yuen for at least the same reasons explained above.

III. Conclusion

For the reasons explained above, all of the pending claims are now in condition for allowance and should be allowed.

Charge any excess fees or apply any credits to Deposit Account No. 50-1078.

Respectfully submitted,

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